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Electronically-tunable Floating Capacitance Simulator with Only VDTAs and a Grounded Capacitor

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Abstract

In this paper, an electronically tunable floating capacitance simulator circuit based on voltage differencing tranconductance amplifiers (VDTAs) is presented. The presented circuit is realized by the employment of only two VDTAs as active elements together with one grounded capacitor as a passive element, without an external passive resistor. The circuit is simple and canonical structure as well as attractive for integration. The resulting equivalent capacitance value of the proposed simulator can be adjusted electronically through the transconductances of the VDTAs. To emphasize the advantage of this circuit, the floating immitance function simulator circuit and active filter realizations are also suggested as application examples. Performance simulations using PSPICE are employed to verify the theoretical analysis.

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Keywords : Voltage Differencing Transconductance Amplifier (CFTA), floating capacitor, immitance function simulator

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1. Introduction

Floating simulator circuits are very useful active building blocks in many applications such as filter design, oscillator design and cancellation of parasitic elements. This is due to the well-known fact that the use of the physical capacitor, particularly of large values, is either not permitted or is unwanted in the integrated circuit technology. Accordingly, several floating capacitance simulator circuits using various active elements were realized in literature [1]-[9]. However, they still suffer from the following weakness:

i) they have either two of more active devices or more than one passive element for floating capacitance simulation [1]-[9].
ii) they use some floating passive components [1], [3], [5].
iii) they employ any external passive resistors [1], [3], [5]-[8].
iv) they cannot be tuned electronically [1], [3], [7].

The voltage differencing transconductance amplifier (VDTA) is a recently introduced active element [10]. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. Therefore, the VDTA device is very suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily [11]. All these advantages make the VDTA an alternative choice for the implementation of voltage-mode analog signal processing circuits.

This work presents a floating capacitance simulator topology employing VDTA as a novel active element. The proposed capacitor is generated with two VDTAs and one grounded capacitor. The proposed floating simulator can be tuned electronically through the transconductance parameter of the VDTA. Since the circuit is composed of only grounded capacitor without requiring any external passive resistor, accordingly, it is a canonical structure and quite suitable for fully integrated circuit design [12]. An application example together with the simulation results are also given to illustrate the performance of the proposed floating simulator circuit.

2. The Concept of VDTA

As symbolically shown in Fig.1, the VDTA device is an active five-terminal building block, when p and n are input terminals, z, +x and -x are output terminals. The terminal relation of this device can be expressed by the following matrix equation [10] :

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad (1)$$

where g_{mF} and g_{mS} are the first and second transconductance gain of the VDTA respectively. From equation (1), the differential input voltage from the terminals *p* and *n* is transformed into output currents at the terminal *z* with first transconductance gain (g_{mF}). The voltage drop at the terminal z (v_z) is transformed into output currents at the terminal *x*+ and *x*- with second transconductance gain (g_{mS}). In general, the transconductance gains of the VDTA are electronically controllable.

Recently, the simple CMOS realization of the VDTA is introduced in [11]. Fig.2 shows the internal structure of the circuit, which is composed of two Arbel-Goldminz transconductances [13]. In this case, the g_{mF}- and g_{mS}– values of this element are determined by the output transistor transconductance, which can respectively be approximated as :

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2} \right) + \left(\frac{g_3 g_4}{g_3 + g_4} \right) \quad (2)$$

and

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right) \tag{3}$$

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$ is the transconductance value of the *i*-th MOS transistor (i = 1, 2, …, 8), I_{Bi} is the bias current, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the *i*-th transistor, respectively.

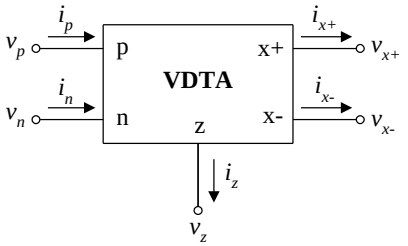

Fig. 1. Electrical symbol of the VDTA

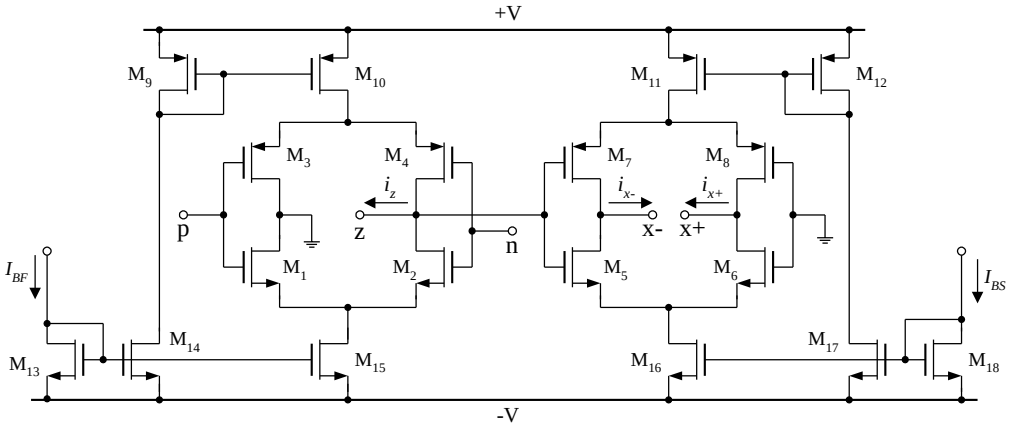

Fig. 2. CMOS implementation of the VDTA

3. Proposed Floating Capacitance Simulator

Fig.3 shows the proposed floating capacitance simulator circuit. It consists of only two VDTA and one grounded capacitor with no external passive resistor requirement; hence, the circuit is simple and canonical structure and very suitable for integrated circuit implementation. Straightforward analysis of the proposed floating inductor in Fig.3 yields the following short-circuit admittance matrix:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{sC_1 g_{mF2} g_{mS2}}{g_{mF1} g_{mS1}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4}$$

or we can obtain the following input impedance :

$$Z_{in} = \frac{g_{mF1} g_{mS1}}{sC_1 g_{mF2} g_{mS2}} = \frac{1}{sC_{eq}} \tag{5}$$

Here, the parameters g_{mFi} and g_{mSi} represent the transconductances g_{mF} and g_{mS} of i-th VDTA (i = 1, 2), respectively. It is clearly seen from above expression that the circuit of Fig.3 can simulate a floating capacitor with an equivalent capacitance value as : $C_{eq} = C_1 g_{mF2} g_{mS2} / g_{mF1} g_{mS1}$. Also note that the value of C_{eq} can be adjusted electronically through either g_{mFi} or g_{mSi} of the i-th VDTA. In addition, if we let $V_1 = 0$ or $V_2 = 0$, then the proposed circuit can be used as a grounded capacitor.

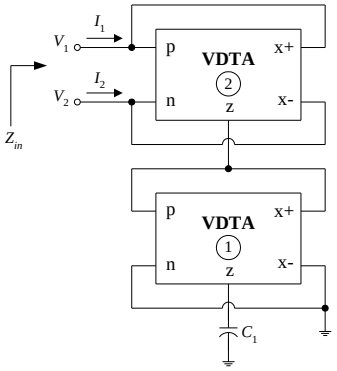

Fig. 3. Proposed floating capacitance simulator topology

4. Performance Verification and Application

The performances of the proposed floating capacitor in Fig.3 has been demonstrated by PSPICE simulation. The simulations were performed by using a CMOS realization as shown in Fig.2 with DC supply voltages equal to ±1.8V. The CMOS transistors in VDTA implementation were simulated using 0.35 μm TSMC CMOS technology process parameters. The dimensions of MOS transistors are given in Table 1.

Table 1. Dimensions of MOS transistors of the VDTA circuit shown in Fig.2.

Transistors	W (μm)	L (μm)
$M_1 – M_2$, $M_5 – M_6$	16.1	0.7
$M_3 – M_4$, $M_7 – M_8$	28	0.7
$M_9 – M_{12}$, $M_{14} – M_{17}$	56	0.7
M_{13} , M_{18}	7	0.7

The proposed floating simulator circuit given in Fig.3 was simulated with C1 = 1 nF. The transconductance values were selected as : gm2 = gmF2 = gmS2 ≅ 0.27 mA/V, and gm1 = gmF1 = gmS1 ≅ 0.27 mA/V, 0.54 mA/V and 0.81 mA/V, which results in : Ceq = 1 nF, 0.25 nF, 0.11 nF, respectively. The impedances of the simulator circuit of Fig.3 relative to frequency is shown in Fig.4. It appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values.

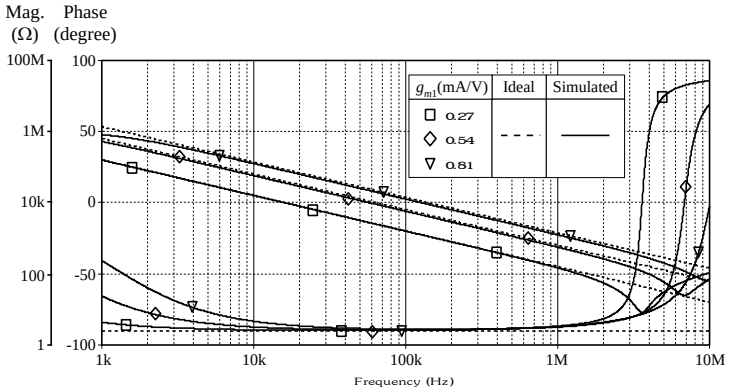

Fig. 4. Ideal and simulated frequency responses of the proposed floating capacitance simulator in Fig.3

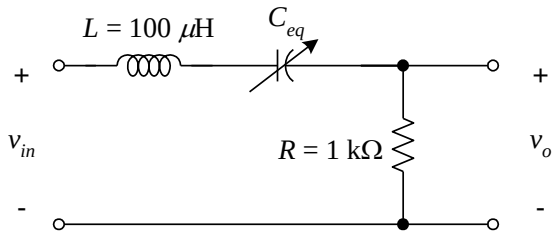

Fig. 5. RLC bandpass filter

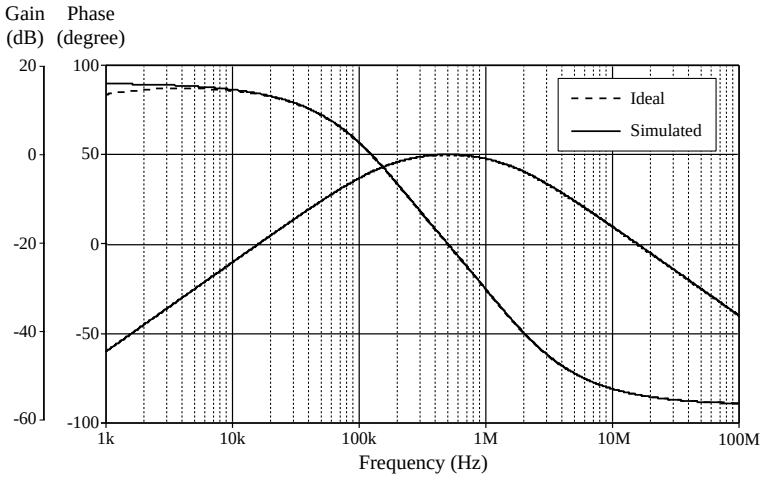

Fig. 6. Ideal and simulated frequency responses of Fig.5

To demonstrate an application of the proposed floating capacitor of Fig.3, it is employed in the RLC bandpass filter as shown in Fig.5. The floating capacitor circuit is simulated with the following component values : C1 = 1 nF and gmF1 = gmS1 = gmF2 = gmS2 ≅ 0.27 mA/V (IBF1 = IBS1 = IBF2 = IBS2 = 20 μA), which results in Ceq = 1 nF. Fig.6 shows the frequency responses of the bandpass filter of Fig.5, which appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values over several decades. Moreover, in order to demonstrate the electronic controllability of the proposed floating capacitor, the value of Ceq in Fig.5 was adjusted to 1 nF, 0.25 nF and 0.11 nF, by changing gmF1 = gmS1 ≅ 0.27 mA/V, 0.54

mA/V and 0.81 mA/V, respectively, while keeping gmF2 = gmS2 constant at 0.27 mA/V. This tuning leads to obtain the center frequency fc ≅ 0.5 MHz, 1 MHz and 1.5 MHz, respectively. The simulated magnitude responses of the bandpass filter in Fig.5 with electronically variable Ceq are depicted in Fig.7. From the results, the corresponding fc are obtained as : 0.49 MHz, 0.94 MHz and 1.39 MHz, respectively.

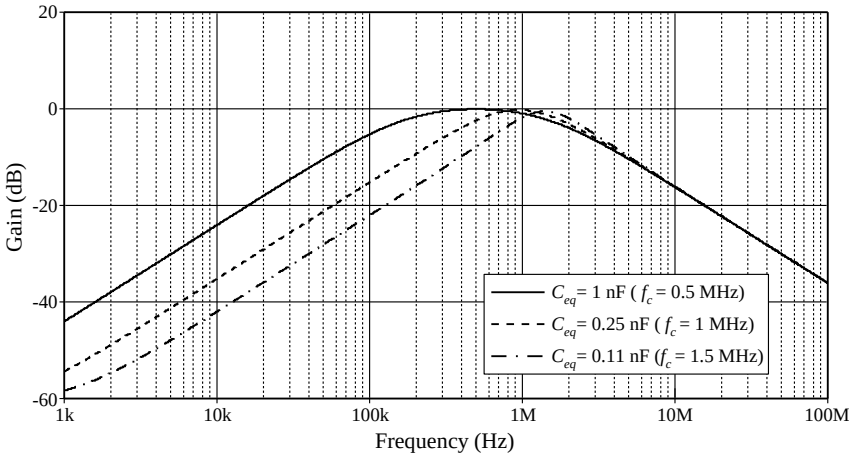

Fig. 7. Simulated magnitude responses of Fig.5 with electronically variable Ceq

5. Conclusion

In this article, floating capacitance simulation scheme is described. The circuit is realized needing two VDTAs and one grounded capacitor, which is suitable for integrated circuit implementation. The value of the simulated capacitance is electronically tunable by adjusting the bias current of the VDTA. The usefulness of the proposed circuit is demonstrated on the RLC bandpass filter design example.

Acknowledgements

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